

Design of Pass Transistor Logic Flip Flop for Low-Power Consumption

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Abstract--In this brief, Pulse-triggered FF (P-FF) is a single-latch structure which is more popular than the conventional transmission gate (TG) and master-slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. The low-power flip-flop (FF) design featuring an explicit type pulse-triggered structure and a modified true single phase clock latch based on a signal feed-through scheme is presented. The proposed design successfully solves the long discharging path problem in conventional explicit type pulse-triggered FF (P-FF) designs and achieves better speed and power performance.

Based on post-layout simulation results using CADENCE VIRTUOSO GPDK CMOS180-nm technology, the proposed design outperforms the conventional PTL-FF design by using only 17 transistors. The average power delay is reduced. In the meantime, the performance edges on power and power-delay-product metrics are 42.7% and 49.7%, respectively.

Index Terms—Flip-flop (FF), low power, pulse triggered.

I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. So this Low Power Pulse Triggered Flip Flop reviews various strategies and methodologies for designing low power circuits and systems. It describes the many issues facing designers at architectural, logic, circuit and device levels and presents some of the techniques that have been proposed to overcome these difficulties. The article concludes with the future challenges that must be met to design low power, high performance systems.

Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs now a-days often adopt intensive pipelining techniques and employ many FF-rich modules such as register file, shift register, and first in-first out. It is also estimated that the power consumption of the clock system, which consists of clock distribution networks and storage elements, is as high as 50% of the total system power. FFs thus contribute a significant portion of the chip area and power consumption to the overall system design.

The term pulse-triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not reflect the input state until the falling edge of the clock pulse. As this kind of flip-flops are sensitive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up prior to the clock pulse's rising edge and must not be changed before the falling edge. Otherwise, ambiguous results will happen.

A P-FF consists of a pulse generator for strobe signals and a latch for data storage. If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master-slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Despite these advantages, pulse generation circuitry requires delicate pulse width control to cope with possible variations in process technology and signal distribution network. In a statistical design framework is developed to take these factors into account. To obtain balanced performance among power, delay, and area, design space exploration is also a widely used technique.

In this brief, we present a novel low-power P-FF design based on a signal feed-through scheme. Observing the delay discrepancy in latching data 1 and 0, the design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass

transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

II. CONVENTIONAL P-FF DESIGNS

PF-FFs, in terms of pulse generation, can be classified as an implicit or an explicit type. In an implicit type P-FF, the pulse generator is part of the latch design and no explicit pulse signals are generated. In an explicit type P-FF, the pulse generator and the latch are separate. Without generating pulse signals explicitly, implicit type P-FFs is in general more power-economical. However, they suffer from a longer discharging path, which leads to inferior timing characteristics. Explicit pulse generation, on the contrary, incurs more power consumption but the logic separation from the latch design gives the FF design a unique speed advantage. Its power consumption and the circuit complexity can be effectively reduced if one pulse generator is shared by a group of FFs (e.g., an n-bit register). In this brief, we will thus focus on the explicit type P-FF designs only.

A. EP-DCO: explicit -Data closed to output Flip-Flop

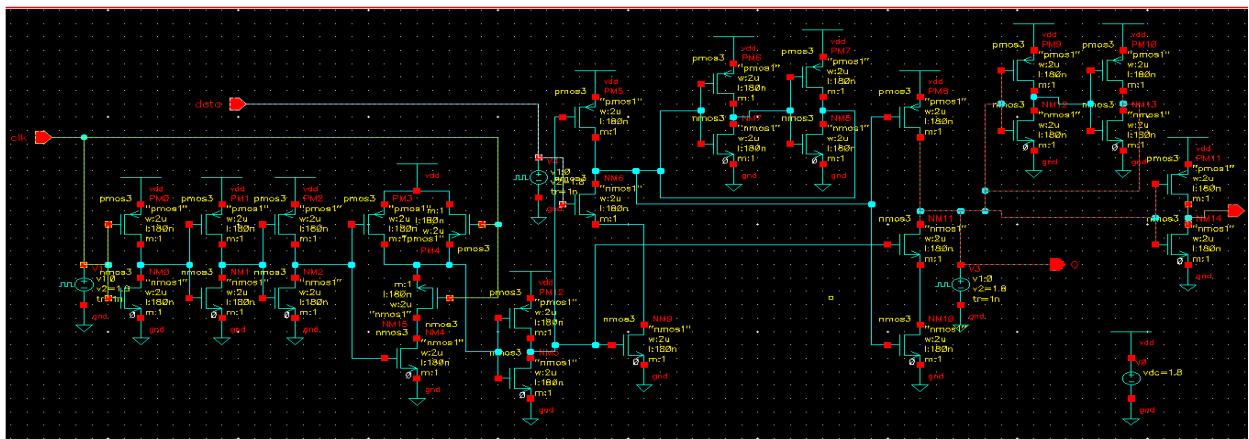


Fig.2.1(a) EP-DCO schematic design in cadence tool

To provide a comparison, some existing P-FF designs are reviewed first. Fig. 2.1(a) shows a classic explicit P-FF design, named data-closed-to-output (ep-DCO). It contains a NAND-logic-based pulse generator and a semi-dynamic true single-phase-clock (TSPC) structured latch design. In this P-FF design, inverters I3 and I4 are used to latch data, and inverters I1 and I2 are used to hold the internal node X. The pulse width is determined by the delay of three inverters. This design suffers from a serious drawback, i.e., the internal node X is discharged on every rising edge of the clock in spite of the presence of a static input "1." This gives rise to large switching power dissipation. To overcome this problem, many remedial measures such as conditional capture, conditional precharge, conditional discharge, and conditional pulse enhancement scheme have been proposed.

B. CDFF: conditional discharged Flip-Flop

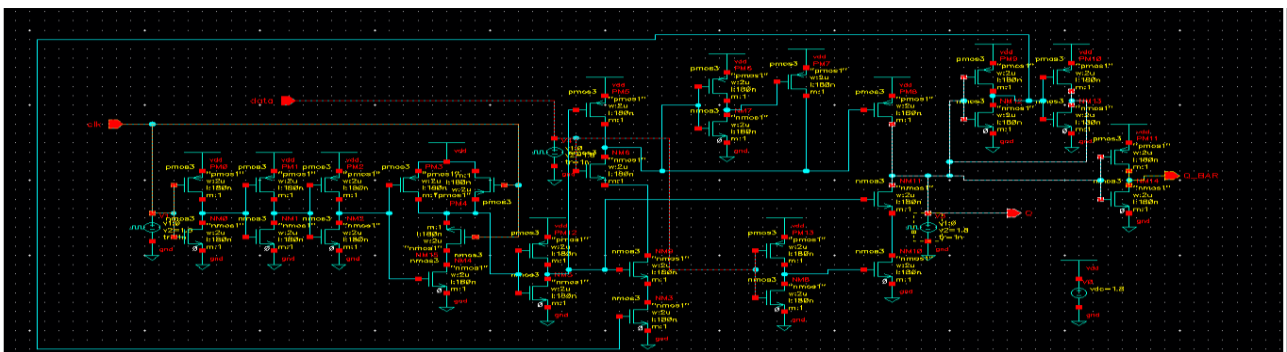


Fig.2.1(b) CDFF schematic design in cadence tool

Fig. 2.1(b) shows a conditional discharged (CD) technique .An extra nMOS transistor MN3 controlled by the output signal Q_{fbk} is employed so that no discharge occurs if the input data remains “1.” In addition, the keeper logic for the internal node X is simplified and consists of an inverter plus a pull-up pMOS transistor only.

C. SCDF: Static- conditional discharged Flip-Flop

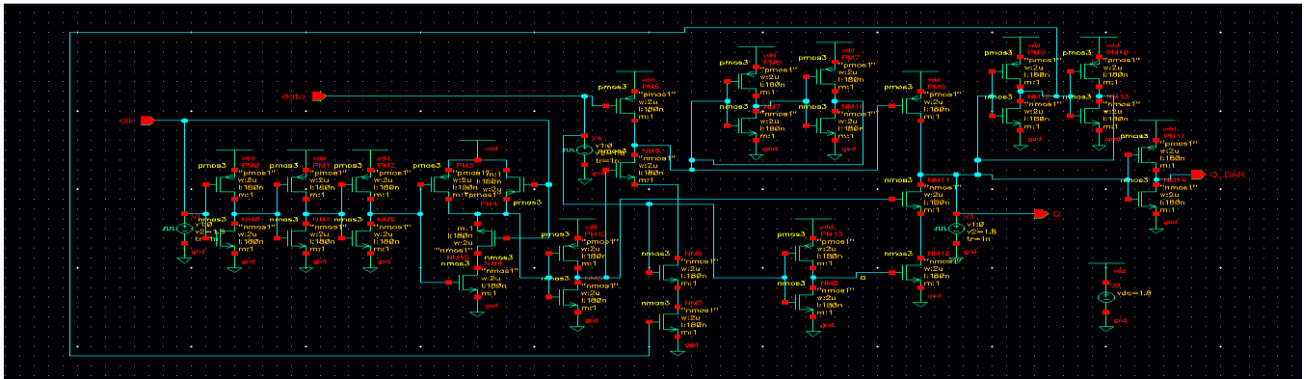


Fig.2.1(c) SCDF schematic design in cadence tool

Fig. 2.1(c) shows a similar P-FF design (SCDF) using a static conditional discharge technique . It differs from the CDF design in using a static latch structure. Node X is thus exempted from periodical precharges. It exhibits a longer data-to-Q (D-to-Q) delay than the CDF design. Both designs face a worst case delay caused by a discharging path consisting of three stacked transistors, i.e., MN1–MN3. To overcome this delay for better speed performance, a powerful pull-down circuitry is needed, which causes extra layout area and power consumption. The modified hybrid latch flip-flop (MHLFF).

D. MHLFF: Modified hybrid latch flip flop

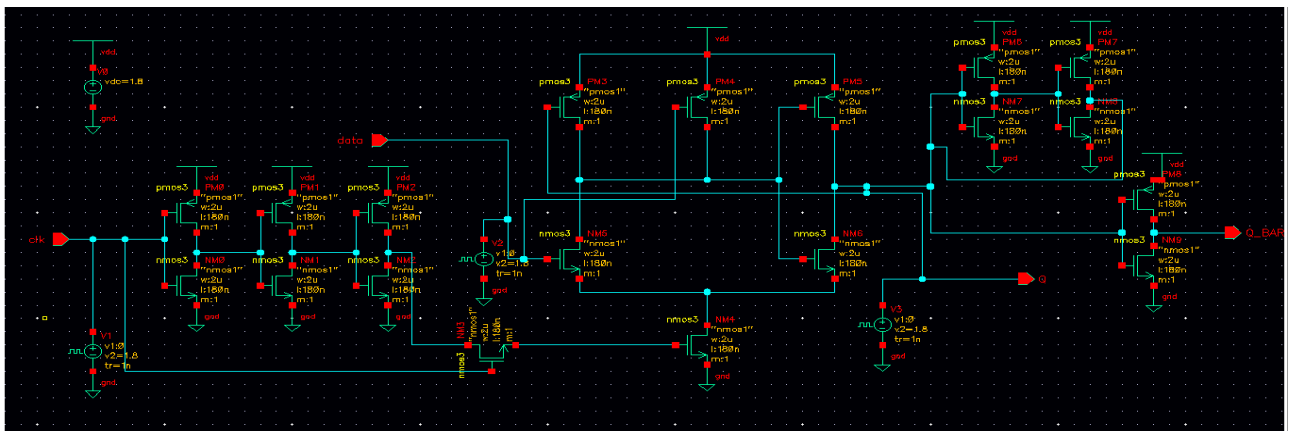


Fig.2.1(d) MHLFF schematic design in cadence tool

Fig. 2.1(d) also uses a static latch. The keeper logic at node X is removed. A weak pull-up transistor MP1 controlled by the output signal Q maintains the level of node X when Q equals 0. Despite its circuit simplicity, the MHLFF design counters two drawbacks. First, since node X is not precharged, a prolonged 0 to 1 delay is expected. The delay deteriorates further, because a level-degraded clock pulse (deviated by one VT) is applied to the discharging transistor MN3. Second, node X becomes floating in certain cases and its value may drift causing extra dc power.

E. TSPCFF: True Single Phase Clock flip flop

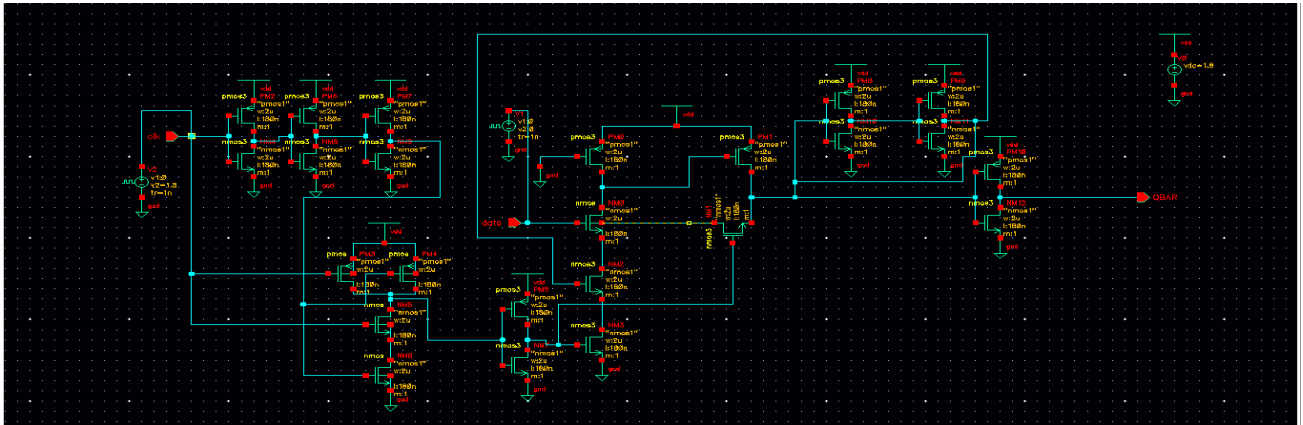


Fig.2.1(e) TSPCFF schematic design in cadence tool

A weak pull-up pMOS transistor MP1 with gate connected to the ground is used in the first stage of the TSPC latch. This gives rise to a pseudo-nMOS logic style design, and the charge keeper circuit for the internal node X can be saved. In addition to the circuit simplicity, this approach also reduces the load capacitance of node X. Second, a pass transistor MNx controlled by the pulse clock is included so that input data can drive node Q of the latch directly (the signal feed-through scheme). Along with the pull-up transistor MP2 at the second stage inverter of the TSPC latch, this extra passage facilitates auxiliary signal driving from the input source to node Q. The node level can thus be quickly pulled up to shorten the data transition delay. Third, the pull-down network of the second stage inverter is completely removed. Instead, the newly employed pass transistor MNx provides a discharging path. The role played by MNx is thus twofold, i.e., providing extra driving to node Q during 0 to 1 data transitions, and discharging node Q during “1” to “0” data transitions. Compared with the latch structure used in SCDF design, the circuit savings of the proposed design include a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a control inverter. The only extra component introduced is an nMOS pass transistor to support signal feedthrough. This scheme actually improves the “0” to “1” delay and thus reduces the disparity between the rise time and the fall time delays.

III. PROPOSED PTL-FF DESIGNS

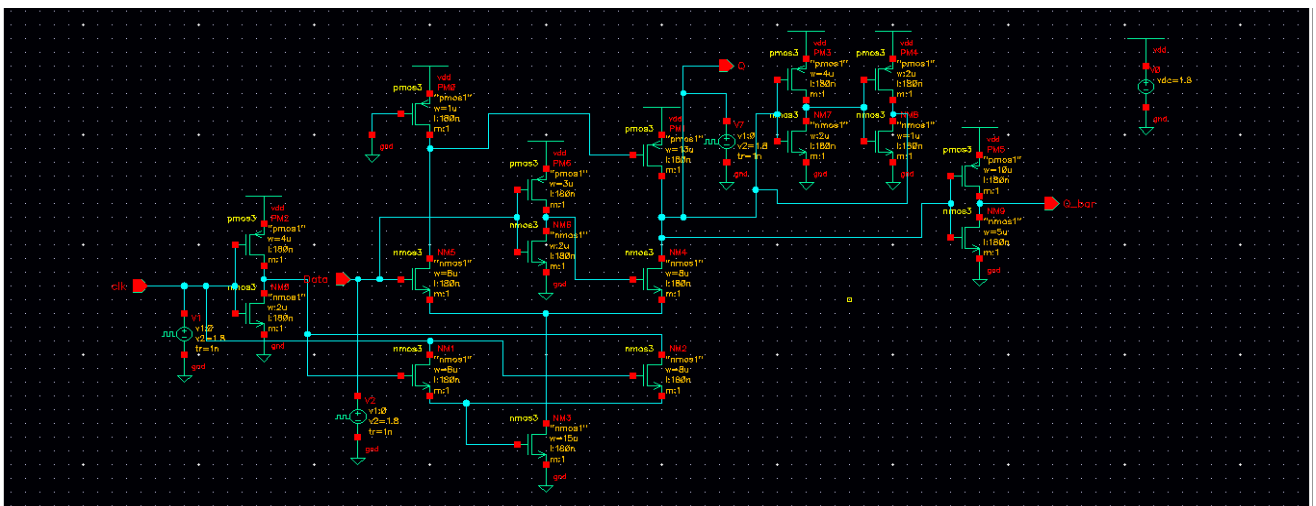


Fig.3.1 proposed PTL-FF schematic design in Cadence tool

The proposed design, as shown in Fig. 2.2, adopts two measures to overcome the problems associated with existing PFF designs. The first one is reducing the number of nMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is “1”. Refer to Fig. 3.1, As opposed to the transistor stacking design in Fig.2.1 (a),(b),(c),(d) and (e), this PFF design discharging path using PTL. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the

discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless. At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N3 can be reduced also.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." It steps in when node X is discharged VTP below the VDD. This provides additional boost to node Z (from VDD-VTH to VDD). The generated pulse is taller, which enhances the pull-down strength of transistor N1.

After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The leads to a better power performance than those schemes using an indiscriminate pulse width enhancement approach. Another benefit of this conditional pulse enhancement scheme is the reduction in leakage power due to shrunken transistors in the critical discharging path and in the delay inverter.

The proposed design is shown in Fig.ref PTLFF. In this proposed design, the pulse generation circuitry is made separately through a 2 input PTL Style AND gate and two inverters. so that it can be used as an explicit pulse generator i.e., the same pulse generator can be shared among multiple flip flops. This sharing can help indistributing the power head of the pulse generator across many explicit flip flops. One input to the PTL Style AND gate is normal clock and the other input is the inverted clock which is taken from clock passed through an inverter. So, the two inputs to the AND gate are mostly complementary except at the rising edge of the clock. So, at every rising edge of the clock a short pulse will be generated during which the latch will be open. In this short pulse the evaluation phase will be completed. Due to this the clock will not have to be high for long periods which reduces the power consumption. P1,P2,N1 and N2 constitute a PTL Style AND gate and if this output is given to an inverter, it totally makes an AND gate. This AND gate output is given to the discharging transistor N4. So, this transistor will be on for the short duration where both the inputs of the AND gate are high which is defined by the delay of the inverter I1. Due to this CMOS logic there will be less leakage as the voltages are maintained at either 0 or 1 but not Vdd-Vth as in PTL logic. Due to this the FF will be a bit faster and also the extra pulse enhancement transistor in Fig.1 can be removed.

The latch part is almost same as that TSPCFF. The latch consists of 13 transistors. Each transistor is having its own use. Instead of using clock for precharging, a small pull-up pMOS transistor P4 is used whose input is continuously grounded. So, node X will be high most of the time. The evaluation path transistor N6 is controlled by the feedback from the output (q fdbk). Therefore, if the state of input data is same as that of output evaluation path will be turned off preventing the discharge at node X. This results in power saving when input data remains idle for more than one clock cycle. Although P4 is statically ON, it will not result in static power dissipation because as soon as the data sampling finishes and 'q' obtains the value of 'data', the pull down path get turned off node X is pulled back to high without any static power being dissipated. There are 3 transistors stacked in the evaluation path which less when compared with other flip flops.

This proposed design will be a bit faster than that of the TSPCFF design as the voltage at node Z will be Vdd during the pulse triggering. The power consumption will be more when compared with a single FF. But, due to sharing the power consumption is reduced in a large extent. When a single pulse generator is shared among FFs the power is almost 50% less than TSPCFF. A system using explicit pulse generator will be definitely power efficient than that using implicit pulse generator. If only the latch is considered 1 transistor is reduced and if complete FF is considered the proposed design contains 3 more transistors. But if the explicit pulse generator is shared among 16 FFs then the total number of transistors reduced is 42. If this sharing increases transistor saving also increases. When it is compared with another explicit pulse triggered FF ep-DCO, it is showing better results. The transistor count is reduced by 6 and it is showing 43% better D-Q delay and a better PDP. These comparisons are shown in the tables and graphs.

IV. RESULTS

SIMULATION OUTPUTS:

The simulation results of above designs are shown below in the Fig. 4(a) to Fig. 4(l). A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run these simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation. To demonstrate post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the 6 P-FF designs shown in Fig. 2.1(a)EPDCO, 2.1(b)CDFF, Fig. 2.1(c)SCDFF, Fig. 2.1(d)MHLFF, Fig. 2.1(e)TSPCFF, 3.1 to the correctness of data capturing as well as the power consumption. All designs are further optimized subject to the tradeoffs between power and D-to-Q delay.

EP-DCO:

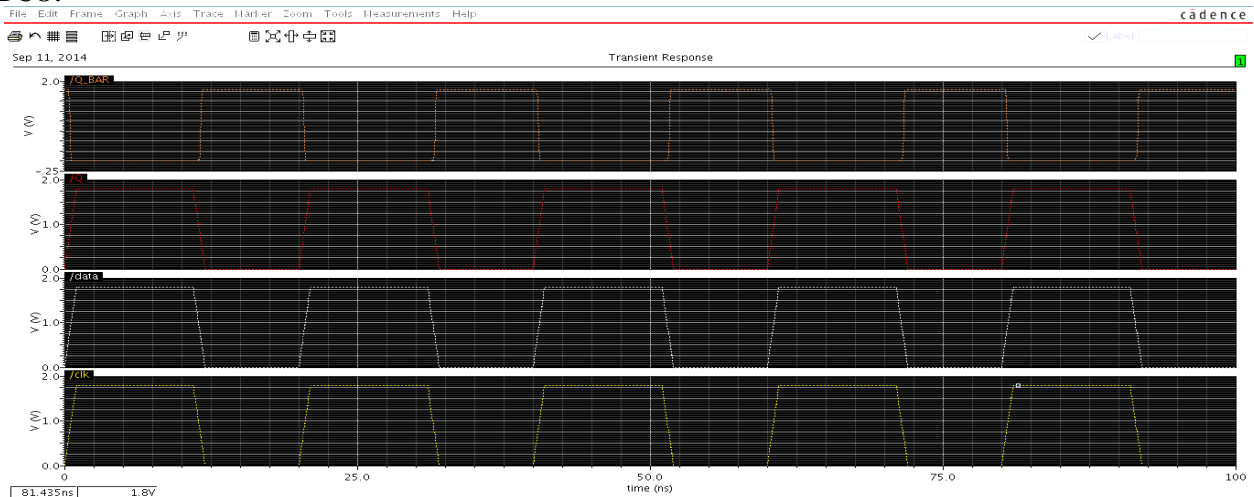


Fig 4(a)-Simulation output EP-DCO using Cadence tool.

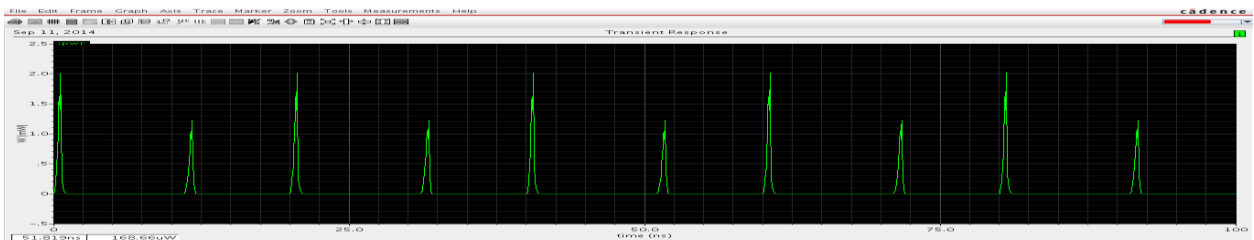


Fig 4(b) Power consumed by EP-DCO using in Cadence tool in 180nm.

CDFF:

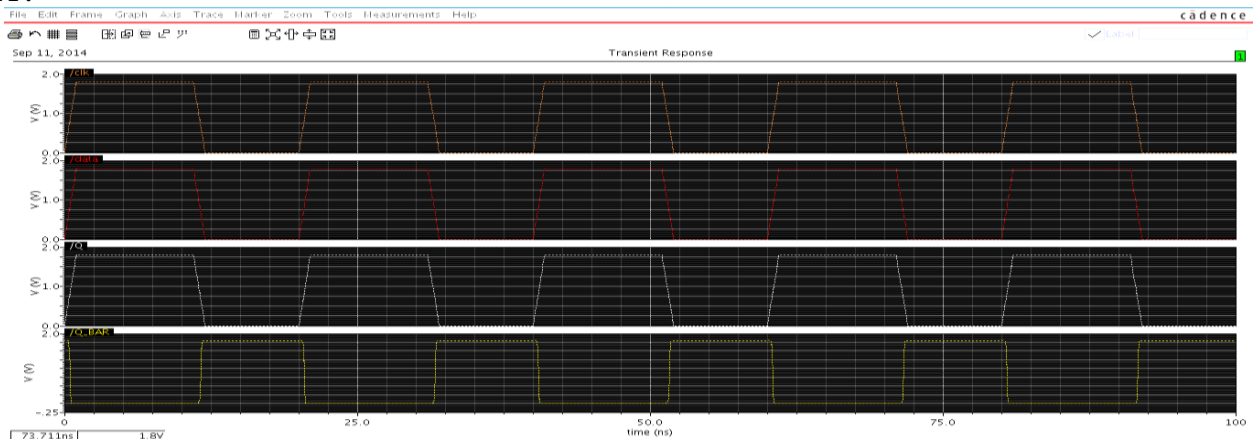


Fig 4(c)Simulation output CDFFF using Cadence Tool.

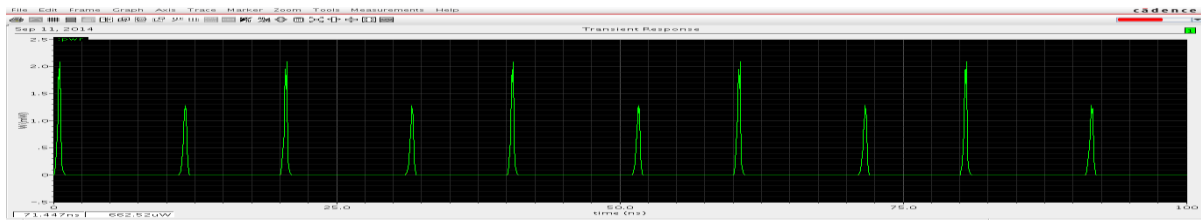


Fig 4(d) Power consumed by CDFFF using in Cadence tool in 180nm.

SCDFF:

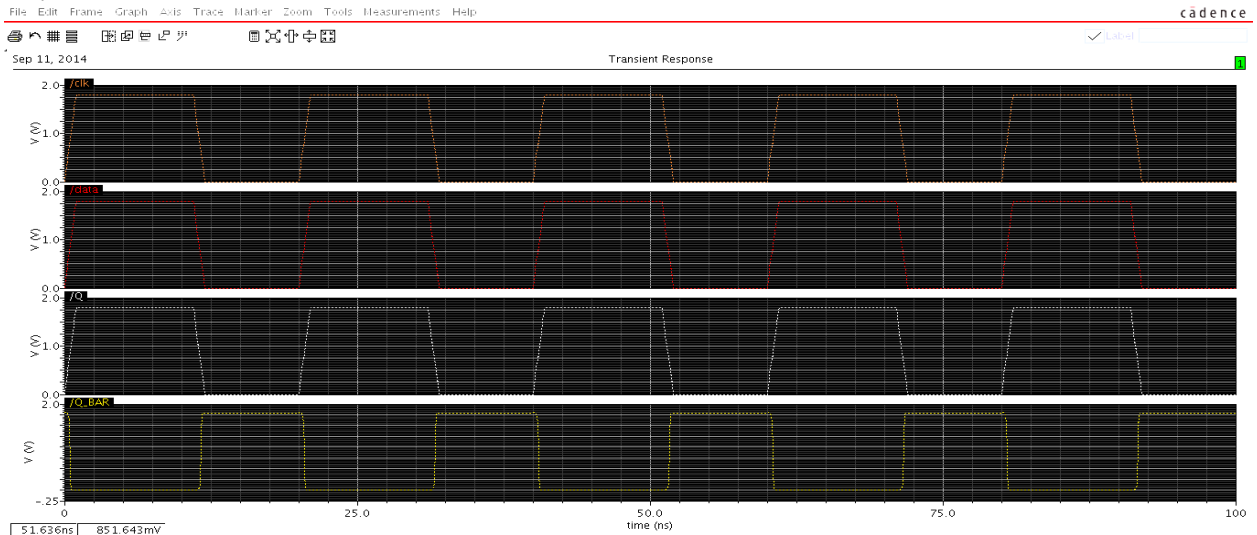


Figure 4(e)Simulation output SCDFF using Cadence Tool.

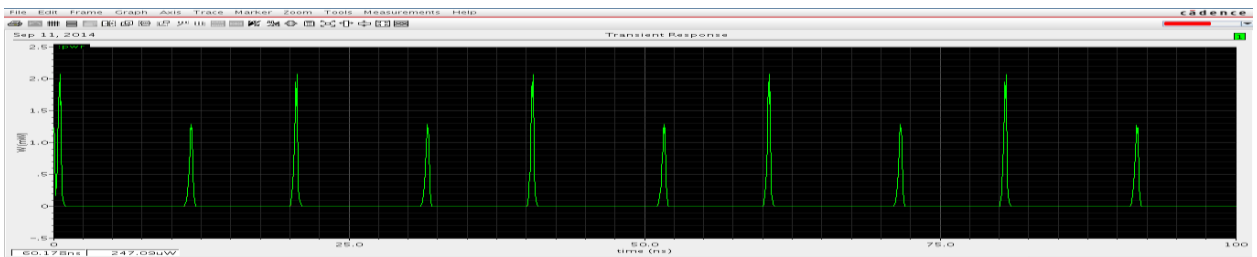


Figure 4(f) Power consumed by CDFFF using in Cadence tool in 180nm.

MHLFF:

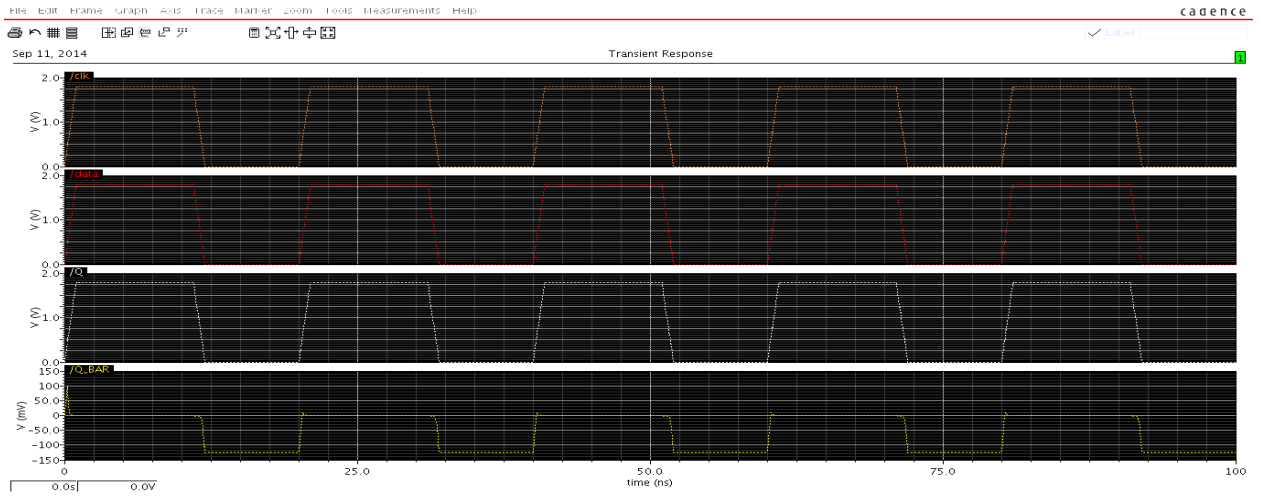


Fig 4(g)Simulation output MHLFF using Cadence Tool.

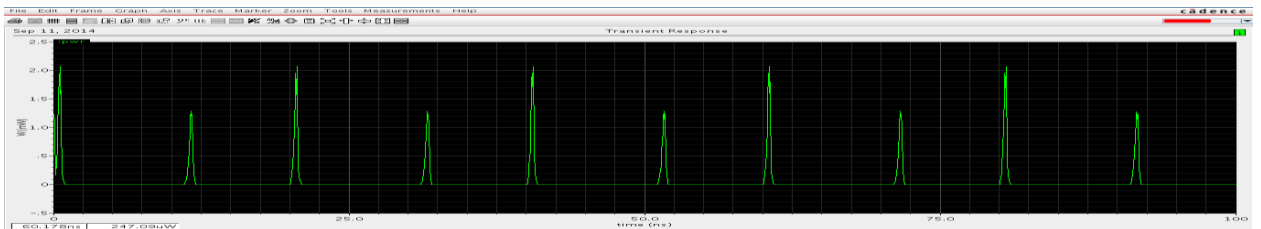


Fig 4(h) Power consumed by MHLFF using in Cadence tool in 180nm.

TSPCFF:

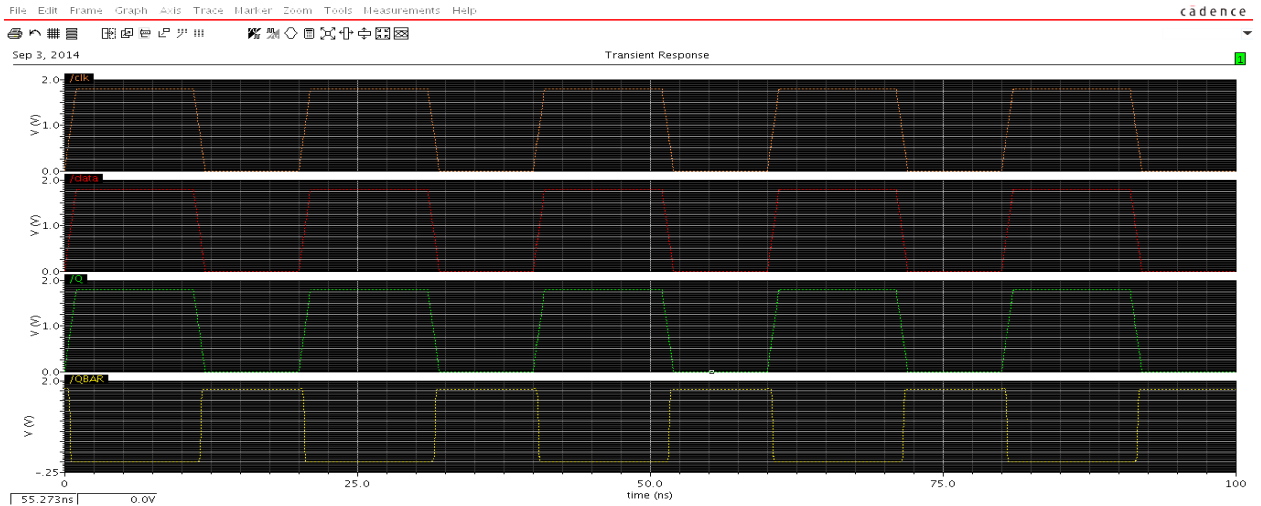


Fig 4(i)Simulation output TSPCFF using Cadence Tool.

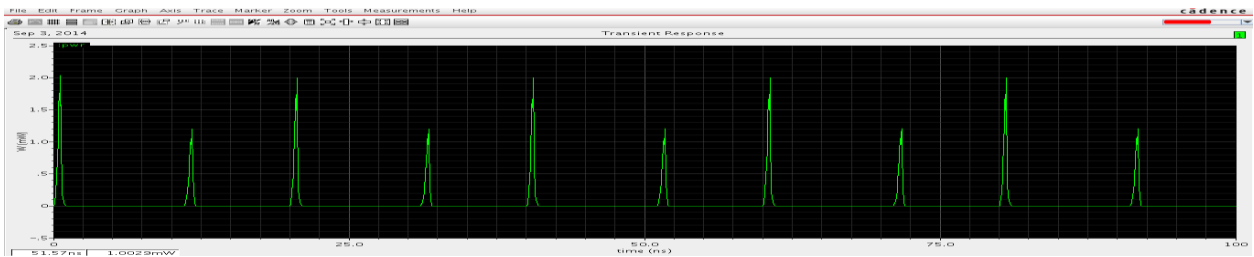


Fig 4 (j)Power consumed by TSPCFF using in Cadence tool in 180nm.

PTLFF:

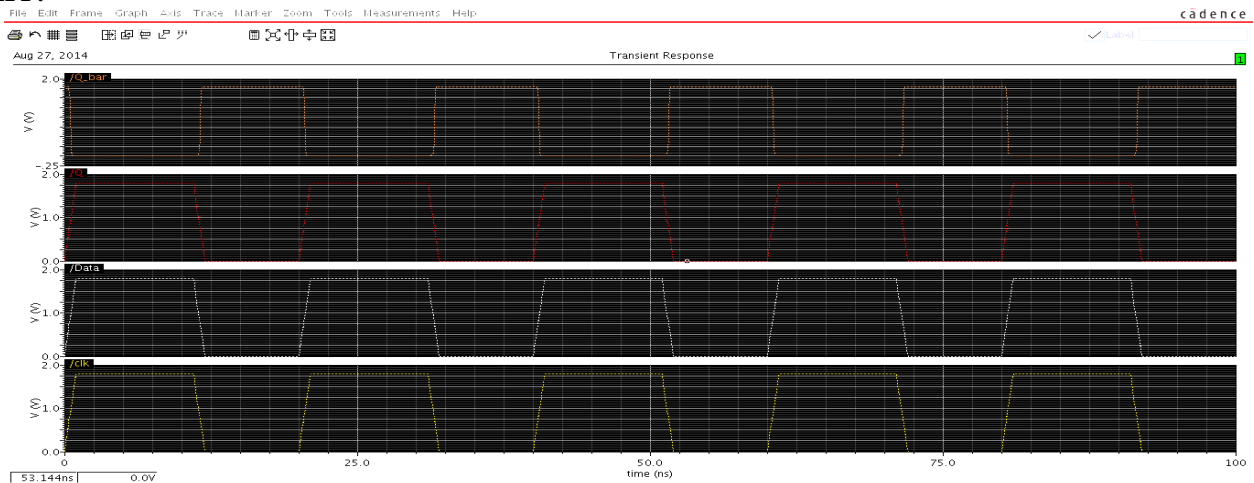


Fig 4(k)Simulation output PTLFF using Cadence Tool.

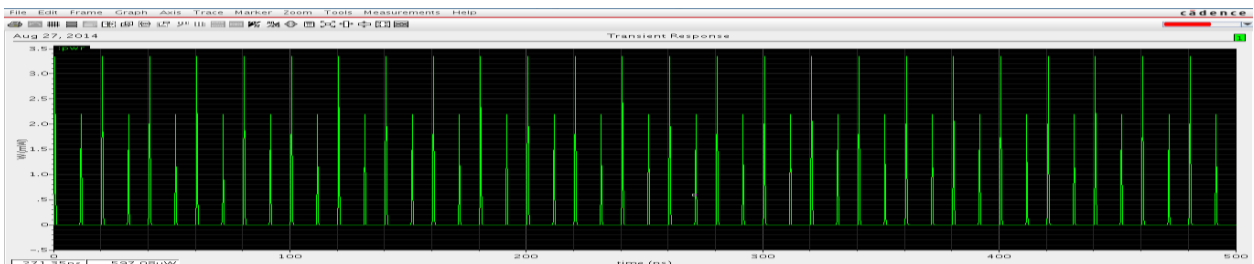


Fig 4 (l)Power consumed by PTLFF using in Cadence tool in 180nm.

The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations. The compared designs include four explicit type P-FF designs shown in Fig. 1, an implicit type P-FF design named SDFF , a TG latch based P-FF design ep-SFF , plus two non-P-FF designs. One of them is a conventional TG master–slave-based FF (TGFF) and the other one is an adaptive-coupling-configured FF design (ACFF) . A conventional CMOS NAND-logic-based pulse generator design with a three-stage inverter chain as show in Fig. 1(a)] is used for all P-FF designs except the MHLFF design, which employs its own pulse generation circuitry as specified in Fig. 2.1(d).

The target technology is the CADENCE VIRTUOSO GPKD 180-nm CMOS process. Since pulse width design is crucial to the correctness of data capture as well as the power consumption, the transistors of the pulse generator logic are sized for a design spec of 120 ps in pulse width in the TT case. The sizing also ensures that the pulse generators can function properly in all process corners. With regard to the latch structures, each P-FF design is individually optimized subject to the product of power and D-to-Q delay. To mimic the signal rise and fall time delays, input signals are generated through buffers. Since the proposed design requires direct output driving from the input source, for fair comparisons the power consumption of the data input buffer (an inverter) is included. The output of the FF is loaded with a 20-fF capacitor. An extra loading capacitance of 3 fF is also placed at the output of the clock buffer. The operating condition used in simulations is 500 MHz/1.0 V.

Table 1. Comparison of various P-FF designs

P-FF(Pulse Trigger Flip Flop)	EP-DCO	SCDFF	CDFF	MHLFF	TSPCFF	Proposed PTL-FF
NO. OF TRANSISTORS	28	31	30	19	24	17
AVG. POWER (μW)	49.99	55.61	54.74	52.39	88.76	49.49
DELAY (ps)	1530	711.69	853.8	615	615	508

V. CONCLUSION

In this Paper, the various Flip flop design like, EP-DCO, MHLFF, SCDFF, CDFF, TSPC based P-FF & Proposed NEW P-FF are discussed. The pulse triggered Flip Flop (P-FF) design by employing two new design measures. The first one successfully reduces the number of transistors stacked along the discharging path by incorporating a PTL based AND logic. The second one supports conditional enhancement to the height and width of the discharging pulse so that the size of the transistors in the pulse generation circuit can be kept minimum. These were been also designed in Cadence & Tanner Tool those result waveforms are also discussed. The comparison table also added to verify the designed methods using the CADENCE VIRTUOSO GPDK 180-nm CMOS technology. With these all results Proposed PTLFF performed speed or power better than EP-DCO, MHLFF, SCDFF, CDFF and TSPCFF designs.

A fundamentally different approach for constructing a FF uses pulse signals. The idea is to construct a short pulse around the rising (or falling) edge of the clock. This pulse acts as the clock input to a latch, sampling the input in a short window. The combination of a pulse-generation circuitry and a latch results in a positive edge triggered register. Pulse triggered FF's reduce the number of latch stages into a single stage. The logic complexity and number of stages are reduced in these pulse triggered FF's leading lesser D-to-Q delays. The main advantage of these pulse triggered FF's is that they allow time borrowing across clock cycle boundaries and feature a zero or even negative setup time. Due to these advantages P-FF's has been considered a popular alternative for traditional master slave FF.

In this brief, we presented a novel P-FF design by employing a modified TSPC latch structure incorporating a mixed design style consisting of a pass transistor and a pseudo-nMOS logic. The key idea was to provide a signal feedthrough from input source to the internal node of the latch, which would facilitate extra driving to shorten the transition time and enhance both power and speed performance. The design was intelligently achieved by employing a simple pass transistor. Extensive simulations were conducted, and the results did support the claims of the proposed design in various performance aspects.

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